

EXHIBIT C

MAR 17 2006

Attorney Docket No. 5649-1235

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re: Tae-joong Song

Serial No.: 10/783,481

Filed: February 20, 2004

For: MEMORY DEVICES HAVING BIT LINE PRECHARGE CIRCUITS WITH OFF
CURRENT PRECHARGE CONTROL AND ASSOCIATED BITLINE
PRECHARGE METHODS

Examiner: Ly D. Pham

Confirmation No.: 1306

Group Art Unit: 2827

Commissioner for Patents

Washington, D.C. 20231

STATEMENT OF ACCURACY OF A TRANSLATION
37 CFR 1.52(d), 37 CFR 1.55(a) AND 37 CFR 1.69

I, the below named translator, hereby state that:

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That I am knowledgeable in the English language and in the language of the

☐ attached document☒ below identified document,

Korean Application Serial No. 2003-36748 as filed on June 9, 2003;

and I believe the attached English translation to be a true and complete translation of this document.

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MEMORY DEVICE HAVING IOFF ROBUST PRECHARGE CONTROL AND BITLINE PRECHARGE METHOD

5 BACKGROUND OF THE INVENTION

1. Field of the Invention

The present invention relates to a semiconductor memory device, and more particularly, to a memory device having an off-current (I_{off}) robust precharge circuit and a bitline precharge method.

10 2. Description of the Related Art

As the semiconductor memory processing technology has been heading for finer technologies, a deep sub-micron process is being developed. As the technologies are moving into the deep sub-micron technology, in order to improve the performance of a transistor, a smaller value of a threshold voltage (V_{th}) is employed. When a threshold voltage is lowered, the saturation current (I_{dsat}) when the transistor is turned on increases. At the same time, the off-current (I_{off}) when the transistor is turned off, that is, a leakage current, also increases. The correlation between the I_{dsat} current and the I_{off} current with respect to the threshold voltage (V_{th}) is shown as the following equation 1:

20

$$I_{ds} = K e^{\frac{(V_{gs} - V_{th})}{nV_T}} (1 - e^{-\frac{V_{ds}}{V_T}}) \dots\dots(1)$$

Here, K denotes a function of the technology, V_T denotes a thermal voltage (KT/q), n denotes a constant defined as $1 + ((\epsilon_{sr}/\epsilon_{ox}) \cdot t_{ox}/D) \square 1.5$, ϵ_{sr} denotes the dielectric constant of a gate oxide film, t_{ox} denotes the thickness of a gate oxide film, and D denotes a channel depletion width.

FIG. 1 is a diagram of a memory cell array provided to explain the impact of a leakage current. Referring to FIG. 1, in the memory cell array 100 memory cells 102, 106, ... are arranged at intersections of first through third wordlines (WL0, WL1, WL2, ...), a bitline (BL) and a complementary bitline (BLB). Assuming that the first wordline (WL0) is enabled such that a first memory cell 102 is activated, data latched in the first memory cell 102 is

transferred to the bitline (BL) and the complementary bitline (BLB). For convenience of explanation, it is assumed that power supply voltage (VDD) in logic level "1" is stored in a first node (NA) and ground voltage (VSS) in logic level "0" is stored in a second node (NB).

5 Then, data in the first memory cell 102 experiences charge sharing such that a voltage difference between the bitline (BL) and the complementary bitline (BLB) occurs (evaluation). Referring to FIG. 1, the bitline (BL) moves toward the power supply voltage (VDD) level and the complementary bitline (BLB) moves toward the ground voltage (VSS) level such that a voltage
10 difference occurs. This voltage difference is sensed and amplified by a sense amplifier (not shown) so that memory cell data can be determined.

Referring to FIG. 1, memory cells 104 and 106 connected to the second and third wordlines (WL1, WL2) are inactivated such that they are not connected to the bitline (BL) or the complementary bitline (BLB). However, the
15 cell-off-current (Ioff) of the memory cells 104 and 106, that is, a leakage current, flows from the bitline (BL) into memory cell transistors 104 and 106 storing logic zeros such that the power supply voltage level of the bitline (BL) is lowered. Accordingly, the voltage difference of the bitline (BL) and the complementary bitline (BLB) decreases and causes a problem that the sensing speed of the
20 sense amplifier is slowed down.

Meanwhile, the wordlines (WL0, WL1, WL2, ...) are enabled in response to a decoded row address, the bitline (BL) and the complementary bitline (BLB) are precharged to the power supply voltage (VDD) in response to a precharge signal (PRE) and a voltage difference due to the memory cell data
25 occurs and is sensed and amplified by a sense amplifier. Circuit blocks related to these operations are shown in FIG. 2.

Referring to FIG. 2, the blocks include a memory cell array block 100, a row decoder 210, a pre-address decoding circuit and control signal generation unit 220, a bitline precharge unit 230, and a sense amplifier 240. The row
30 decoder 210 and the pre-address decoding circuit 220 relate to operations for enabling wordlines (WL0, ..., WLn), and the bitline precharge circuit 230 responding to a precharge signal (PRE) relates to operations to precharge the

bitline (BL) and the complementary bitline (BLB) to the power supply voltage (VDD) level. The sense amplifier 240 senses and amplifies the bitline (BL) and the complementary bitline (BLB) in which a voltage difference occurs in response to a sensing enable signal (SENSE).

5 FIG. 3 is a diagram explaining the operational timing of the circuit of FIG. 2. Referring to FIG. 3, intervals (a) through (b) are shown. In interval (a), in response to the precharge signal (PRE) in a logic "low" level, the bitline (BL) and the complementary bitline (BLB) are precharged to the power supply voltage (VDD) level. Interval (b) is a floating interval after the precharge signal
10 (PRE) is transited to a logic "high" level and disabled, and before the wordline (WL0) is enabled. In interval (c), wordline (WL0) is transited to a logic "high" level and enabled and due to the memory cell data a voltage difference between the bitline (BL) and the complementary bitline (BLB) occurs, and a sensing enable signal (SENSE) is transited to a logic "high" level and enabled such that
15 the voltage difference between the bitline (BL) and the complementary bitline (BLB) is sensed and amplified. In interval (d), the precharge signal (PRE) is transited to a logic "low" level and enabled such that the bitline (BL) and the complementary bitline (BLB) are precharged to the power supply voltage (VDD) level.

20 Here, in interval (b), before the wordline (WL0) is enabled, the voltage levels of the bitline (BL) and the complementary bitline (BLB), which are precharged to the power supply voltage (VDD) level, are lowered due to the effect of the cell-off-current (I_{off}) described above referring to FIG. 1. Accordingly, it takes a predetermined time more to arrive at the voltage
25 difference of the bitline (BL) and the complementary bitline (BLB) that can be sensed by the sense amplifier. This works as a factor preventing a high speed operation of the memory device.

 Therefore, a memory device, which removes the floating interval such as the interval (b) being affected by the cell-off-current (I_{off}) so that the high
30 speed operation of the memory device is not prevented, is needed.

SUMMARY OF THE INVENTION

The present invention provides a memory device having a cell-off-current robust precharge control circuit.

The present invention also provides a cell-off-current robust precharge method.

5 According to an aspect of the present invention, there is provided a memory device comprising: a plurality of memory cells arranged in rows and columns; a row decoder which decodes a received address signal and enables wordlines of the memory cells; a precharge control circuit which generates a precharge signal in response to a precharge enable signal and a precharge
10 delay signal which is obtained by delaying the precharge enable signal for a predetermined time; and a precharge unit which in response to the precharge signal precharges a bitline and a complementary bitline, wherein the precharge signal is disabled after the wordline is enabled.

It is preferable that the precharge control circuit comprises: a delay
15 circuit unit which receives the precharge enable signal and delays for the predetermined delay time; a NAND gate which receives the precharge enable signal and the output of the delay circuit unit; and an inverter which inverts the output of the NAND gate. The delay time is a time taken for enabling the wordline from a time when the decoded row addresses are transited. The
20 precharge unit comprises: first and second transistors which in response to the precharge signal precharge the bitline and the complementary bitline, respectively, to a power supply voltage level; and a third transistor which in response to the precharge signal equalizes the bitline and the complementary bitline. The first through third transistors are PMOS transistors.

25 According to another aspect of the present invention, there is provided a memory device comprising: a plurality of memory cells arranged in rows and columns; a row decoder which decodes a received address signal and enables wordlines of the memory cells; a precharge control circuit which generates a precharge signal in response to the decoded address signal and a precharge
30 enable signal; and a precharge unit which in response to the precharge signal precharges a bitline and a complementary bitline, wherein the precharge signal is disabled after the wordline is enabled.

It is preferable that the precharge control circuit comprises: a NOR gate which receives the decoded address signals; a first inverter which inverts the output of the NOR gate; a NAND gate which receives the output of the first inverter and the precharge enable signal; and a second inverter which inverts the output of the NAND gate and generates the precharge signal.

According to still another aspect of the present invention, there is provided a method for precharging bitlines of memory cells comprising: decoding received address signals; generating a precharge signal in response to a precharge enable signal and a precharge delay signal obtained by delaying the precharge enable signal for a predetermined time; precharging a bitline and a complementary bitline in response to the precharge signal; and enabling a wordline in response to the decoded address signal, wherein the precharge signal is disabled after the wordline is enabled.

According to yet still another aspect of the present invention, there is provided a method for precharging bitlines of memory cells comprising: decoding received address signals; generating a precharge signal in response to the decoded address signal and a precharge enable signal; precharging a bitline and a complementary bitline in response to the precharge signal; and enabling a wordline in response to the decoded address signal, wherein the precharge signal is disabled after the wordline is enabled.

Accordingly, since the circuit enables wordlines and then disables a precharge signal, the circuit is not affected by an off-current (I_{off}) and greatly increases the voltage difference between a bitline and a complementary bitline such that a sensing margin increases.

BRIEF DESCRIPTION OF THE DRAWINGS

The above objects and advantages of the present invention will become more apparent by describing in detail preferred embodiments thereof with reference to the attached drawings in which:

FIG. 1 is a diagram explaining a typical memory cell array;

FIG. 2 is a diagram showing a circuit included in a prior art memory

device;

FIG. 3 is a diagram explaining the operational timing of the memory device of FIG. 2;

FIG. 4 is a diagram explaining the concept of the present invention;

5 FIG. 5 is a diagram explaining a memory device according to a preferred embodiment of the present invention;

FIG. 6 is a diagram explaining the operational timing of the memory device of FIG. 5;

10 FIG. 7 is a diagram explaining the simulation result of the present invention; and

FIG. 8 is a diagram explaining the simulation result of the prior art memory device as a comparison example of FIG. 1.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

15 Referring to FIG. 4, in a method to generate a precharge signal (PRE) a precharge signal (PRE) is inactivated a predetermined time (ΔT) after a time when a precharge enable signal (PRE_EN) is inactivated, and the precharge signal (PRE) is activated at a time when the precharge enable signal (PRE_EN) is activated. That is, according to a delay circuit 410 (???) inputting a
20 precharge enable signal (PRE_EN), a precharge enable signal (PRE_EN) which is delayed for a predetermined time (ΔT) is generated. The delayed precharge enable signal (PRE_EN) and the precharge enable signal (PRE_EN) are input to a NAND gate 420, and the output of the NAND gate 420 is input to an inverter 430 and is output as a precharge signal (PRE).

25 In relation to the operation of a precharge circuit 230 in the prior art memory device of FIG. 2 responding to a precharge signal (PRE), the concept of the present invention will now be explained in detail.

The precharge circuit 230 of FIG. 2 comprises first and second PMOS transistors 232 and 234, which precharge the bitline (BL) and the
30 complementary bitline (BLB) to the power supply voltage (VDD) level in response to the precharge signal (PRE), and a third PMOS transistor 236 which equalizes the bitline (BL) and the complementary bitline (BLB) to the power

supply voltage (VDD) level in response to the precharge signal (PRE). The precharge circuit 230 precharges the bitline (BL) and the complementary bitline (BLB) to the power supply voltage (VDD) level in response to a logic "low" level of the precharge signal (PRE), and disables the precharge operation of the bitline (BL) and the complementary bitline (BLB) by the precharge signal (PRE) in a logic "high" level.

In response to the precharge enable signal (PRE_EN) in a logic "low" level commanding a bitline precharge operation, the output of the NAND gate 420 is generated as a logic "high" level signal and the precharge signal (PRE) is generated as a logic "low" level signal.

In response to the precharge signal (PRE) in a logic "low" level, the bitline (BL) and the complementary bitline (BLB) are precharged to the power supply voltage (VDD) level. Then, a predetermined time (ΔT) of the delay circuit 410 after a time when the precharge enable signal (PRE_EN) is transited to a logic "high" level, the output of the NAND gate 420 is generated as a logic "low" level signal and the precharge signal (PRE) in a logic "high" level is generated. In response to the precharge signal (PRE) in a logic "high" level, PMOS transistors 232, 234 and 236 of the precharge circuit 230 are turned off and the precharge operation of the bitline (BL) and the complementary bitline (BLB) is disabled.

Here, the predetermined time (ΔT) is a time taken for enabling a wordline in response to decoded row addresses, that is, a time taken for enabling a wordline from a time when row addresses are transited. This is a time set to disable the precharge operation after the wordline is enabled.

FIG. 5 is a diagram explaining a memory device according to a preferred embodiment of the present invention. Referring to FIG. 5, the memory device 500 comprises a memory cell array block 100, a row decoder 210, a pre-address decoding circuit and control signal generation unit 220, a bitline precharge unit 230, and a sense amplifier 240, as in FIG. 2, and further comprises a precharge control circuit unit 510.

The precharge control circuit unit 510 comprises a NOR gate 512 which receives decoded row addresses provided by the pre-decoding circuit 220, a

first inverter 514 which receives the output of the NOR gate 512, a NAND gate 516 which receives the output of the first inverter 514 and a precharge enable signal (PRE_EN), and a second inverter 518 which inverts the output of the NAND gate 516 and generates a precharge signal (PRE).

5 The NOR gate 512 in response to the transition of the decoded row addresses to a logic "high" level generates the output in a logic "low" level, and in response to the precharge enable signal (PRE_EN) generates a precharge signal (PRE). If the precharge enable signal (PRE_EN) is in a logic "low" level, the precharge signal (PRE) is generated in a logic "low" level and precharges
10 the bitline (BL) and the complementary bitline (BLB). Meanwhile, if the precharge enable signal (PRE_EN) is in a logic "high" level, the precharge signal (PRE) is generated in a logic "high" level and disables the precharge operation of the bitline (BL) and the complementary bitline (BLB).

 If the decoded row addresses are in a logic "low" level, the NOR gate
15 512 generates an output signal in a logic "high" level and the precharge signal (PRE) is generated in a logic "low" level. This is to precharge the bitline (BL) and the complementary bitline (BLB) during a time when wordlines (WL0, ..., WLn) are not enabled.

 FIG. 6 is a diagram explaining the operational timing of the memory
20 device of FIG. 5. Referring to FIG. 6, compared to the timing diagram of FIG. 3, the timing diagram includes intervals (a), (c) and (d) and there is no interval (b). In interval (a), in response to the precharge signal (PRE) in a logic "low" level, the bitline (BL) and the complementary bitline (BLB) are precharged to the power supply voltage (VDD) level. In interval (c), after the wordline (WL0) is
25 enabled to a logic "high" level, the precharge signal (PRE) in response to this is transitioned to a logic "high" level and disabled. According to data of a memory cell connected to the enabled wordline (WL0), the bitline (BL) and the complementary bitline (BLB) experience charge sharing and the voltage difference between the bitline (BL) and the complementary bitline (BLB)
30 increases. In response to the sensing enable signal (SENSE) the voltage difference between the bitline (BL) and the complementary bitline (BLB) is sensed and amplified. In interval (d) wordline (WL0) is disabled and in

response to the precharge signal (PRE) in a logic "low" level, the bitline (BL) and the complementary bitline (BLB) are again precharged.

FIG. 7 is a diagram explaining the simulation result of the memory device of the present embodiment. Referring to FIG. 7, in response to the decoded address signal, wordline (WL) is transited to a logic "high" level and enabled, and after a predetermined time, the precharge signal (PRE) is transited to a logic "high" level and disabled. From a time when the wordline (WL) is enabled, the voltage difference of the bitline (BL) and the complementary bitline (BLB) is slowly generated, and at a time when the precharge signal (PRE) is disabled, the voltage difference of the bitline (BL) and the complementary bitline (BLB) increases more. Accordingly, since the voltage difference of the bitline (BL) and the complementary bitline (BLB) is big enough, the sensing margin can be made greater during an activated interval of the sensing enable signal (SENSE) where the voltage difference of the bitline (BL) and the complementary bitline (BLB) is sensed and amplified.

Compared to this, FIG. 8 is a diagram showing the simulation result of the prior art memory device of FIG. 2. Referring to FIG. 8, as described above referring to FIG. 3, the precharge signal (PRE) is transited to a logic "high" level and disabled, and after a predetermined time, the wordline (WL) is transited to a logic "high" level and enabled. At a time when the precharge signal (PRE) is disabled, the voltage difference of the bitline (BL) and the complementary bitline (BLB) begins to take place. Here, due to the effect of the cell off current (I_{off}), the bitline moves toward a logic "low" level and the complementary bitline (BLB) moves toward a logic "high" level which are opposite directions of expected normal voltage levels. Then, a predetermined time delay after a time when the wordline (WL) is enabled, the direction of the bitline (BL) movement is reversed toward a logic "high" level and the direction of the complementary bitline (BLB) movement is reversed toward a logic "low" level and the voltage difference increases. Accordingly, since the voltage difference of the bitline (BL) and the complementary bitline (BLB) is not big enough, there is a problem that during an activated interval of the sensing enable signal (SENSE) where the voltage difference of the bitline (BL) and the complementary bitline (BLB) is sensed and

amplified, the sensing margin decreases.

The method for enabling the wordline (WL) and then disabling the precharge signal (PRE) according to the present embodiment causes current consumption during a time from enabling the wordline (WL) to disabling the precharge signal (PRE), due to formation of a current path between the power supply voltage that is the bitline precharge voltage, and the memory cell data in a logic "low" level. However, the method has advantage that without being effected by the cell-off-current (I_{off}), the voltage difference of the bitline (BL) and the complementary bitline (BLB) can be greatly increased.

Optimum embodiments have been explained above and are shown. However, the present invention is not limited to the preferred embodiment described above, and it is apparent that variations and modifications by those skilled in the art can be effected within the spirit and scope of the present invention defined in the appended claims. Therefore, the scope of the present invention is not determined by the above description but by the accompanying claims.

What is claimed is

1. A memory device comprising:
 - a plurality of memory cells arranged in rows and columns;
 - a row decoder which decodes a received address signal and enables
 - 5 wordlines of the memory cells;
 - a precharge control circuit which generates a precharge signal in response to a precharge enable signal and a precharge delay signal which is obtained by delaying the precharge enable signal for a predetermined time; and
 - a precharge unit which in response to the precharge signal precharges
 - 10 a bitline and a complementary bitline, wherein the precharge signal is disabled after the wordline is enabled.
2. The memory device of claim 1, wherein the precharge control circuit comprises:
 - 15 a delay circuit unit which receives the precharge enable signal and delays for the predetermined delay time;
 - a NAND gate which receives the precharge enable signal and the output of the delay circuit unit; and
 - an inverter which inverts the output of the NAND gate.
 - 20
3. The memory device of claim 2, wherein the delay time is a time taken for enabling the wordline from a time when the decoded row addresses are transited.
- 25 4. The memory device of claim 2, wherein the precharge unit comprises:
 - first and second transistors which in response to the precharge signal precharge the bitline and the complementary bitline, respectively, to a power supply voltage level; and
 - a third transistor which in response to the precharge signal equalizes
 - 30 the bitline and the complementary bitline.

5. The memory device of claim 4, wherein the first through third transistors are PMOS transistors.

6. A memory device comprising:

- 5 a plurality of memory cells arranged in rows and columns;
a row decoder which decodes a received address signal and enables wordlines of the memory cells;
a precharge control circuit which generates a precharge signal in response to the decoded address signal and a precharge enable signal; and
10 a precharge unit which in response to the precharge signal precharges a bitline and a complementary bitline, wherein the precharge signal is disabled after the wordline is enabled.

7. The memory device of claim 6, wherein the precharge control circuit
15 comprises:

- a NOR gate which receives the decoded address signals;
a first inverter which inverts the output of the NOR gate;
a NAND gate which receives the output of the first inverter and the precharge enable signal; and
20 a second inverter which inverts the output of the NAND gate and generates the precharge signal.

8. The memory device of claim 7, wherein the precharge unit comprises:

- first and second transistors which in response to the precharge signal
25 precharge the bitline and the complementary bitline, respectively, to a power supply voltage level; and
a third transistor which in response to the precharge signal equalizes the bitline and the complementary bitline.

30 9. The memory device of claim 8, wherein the first through third transistors are PMOS transistors.

10. A method for precharging bitlines of memory cells comprising:
decoding received address signals;
generating a precharge signal in response to a precharge enable signal
and a precharge delay signal obtained by delaying the precharge enable signal
5 for a predetermined time;
precharging a bitline and a complementary bitline in response to the
precharge signal; and
enabling a wordline in response to the decoded address signal, wherein
the precharge signal is disabled after the wordline is enabled.

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11. A method for precharging bitlines of memory cells comprising:
decoding received address signals;
generating a precharge signal in response to the decoded address
signal and a precharge enable signal;
15 precharging a bitline and a complementary bitline in response to the
precharge signal; and
enabling a wordline in response to the decoded address signal, wherein
the precharge signal is disabled after the wordline is enabled.

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Abstract of the Disclosure

A memory device having an off-current (I_{off}) robust precharge control circuit and a bitline precharge method are provided. The precharge control circuit comprises a delay circuit unit which receives the precharge enable signal and delays for the predetermined delay time; a NAND gate which receives the precharge enable signal and the output of the delay circuit unit; and an inverter which inverts the output of the NAND gate. Accordingly, since the circuit enables wordlines and then disables a precharge signal, the circuit is not affected by an off-current (I_{off}) and greatly increases the voltage difference between a bitline and a complementary bitline such that a sensing margin increases.